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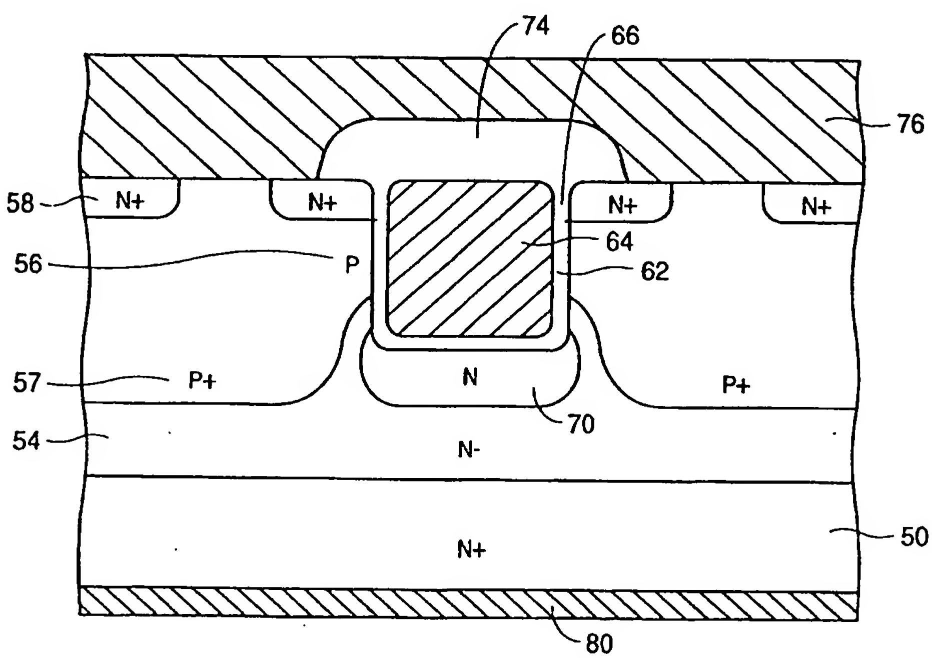
(54) Title: HIGH DENSITY TRENCH DMOS TRANSISTOR WITH TRENCH BOTTOM IMPLANT



(57) Abstract

A trenched DMOS transistor overcomes the problem of a parasitic JFET at the trench bottom (caused by deep body regions (57) extending deeper than the trench) by providing a doped trench (62) and extending into the surrounding drift region (54). This trench bottom implant region (70) has the same doping type, but is more highly doped, than the surrounding drift region (54). The trench bottom implant region (70) significantly reduces the parasitic JFET resistance by optimizing the trench bottom implant dose, without creating reliability problems.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/12046

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 29/76
US CL :257/328, 329, 330
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/328, 329, 330

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,442,214 A (YANG) 15 AUGUST 1995 (15/08/95), COLUMN 3, LINES 1-68.	8-11
Y, P	US 5,558,313 A (HSHIEH ET AL.) 24 SEPTEMBER 1996 (24/09/96) , COLUMN 4, LINES 38-67.	1-7, 12-17
Y	US 4,893,160 A (BLANCHARD) 09 JANUARY 1990 (09/01/90), COLUMN 3, LINES 9-23.	8-11
Y	US 4,964,080 A (TZENG) 16 OCTOBER 1990(16/10/90), COLUMN 6, LINES 35-68.	1-7, 12-17
Y	JP 405,343,691 A 24 DECEMBER 1993 (24/12/93), CONSTITUTION.	1-7, 12-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 OCTOBER 1997	30 OCT 1997

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/12046

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I, claim(s)1-7 and 12-17, drawn to a device, class 257, subclass 328.
Group II, claim(s) 8-11, drawn to a method, class 438, subclass 15+.

The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention could be made by processes materially different from those of the group II invention. For example, diffusing through a bottom of the trench instead of implanting through a bottom of the trench may be performed and the same structure would result.

HIGH DENSITY TRENCH DMOS TRANSISTOR WITH TRENCH BOTTOM IMPLANT

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to transistors and more specifically to a high density trenched DMOS transistor.

Description of the Prior Art

DMOS (diffused metal oxide semiconductor) transistors are well known. Typically these transistors are used in integrated circuits or for power transistors. Some DMOS transistors are trenched transistors; a conductive gate electrode, typically polycrystalline silicon (polysilicon), is located in a trench in the transistor substrate, and the sidewalls and bottom of the trench are insulated with silicon dioxide. The trenched structure increases transistor density by reducing the chip surface area consumed by the polysilicon gate of each transistor. Typically such transistors are used in low to medium voltage applications, and each transistor includes a large number (thousands) of cells. Each cell is defined by a source region diffused into the substrate and by the gate electrode trenches.

The provision of the trenches advantageously increases cell density and also reduces the undesirable parasitic JFET (junction field effect transistor) resistance which typically is present between adjacent cells. The parasitic JFET resistance is one component of the total on-state resistance, R_{DSON}, which is characteristic of such transistors in their conductive (on) state; it is desirable to minimize the on-resistance.

the same gate. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain is of relatively high conductivity (is highly doped), thereby substantially reducing the on-resistance of the device without affecting the device breakdown voltage.

Thus as shown in present Figure 1, the Lidow et al. MOSFET is formed in a chip of monocrystalline silicon 20. Two source electrodes 22 and 23 are separated by a metallized gate electrode 24 which is fixed to but spaced apart from the semiconductor device surface by a silicon dioxide layer 25. Each of source electrodes 22 and 23 supply current to a drain electrode 26 which is fixed to the bottom of the wafer. An N- doped epitaxial layer is deposited on N+ doped substrate 20. P+ doped regions 30 and 31 each include a curved lower portion which serves as a deep body region. Two N+ regions 32 and 33 are formed at the source electrodes 22 and 23 respectively and define, with the P doped regions 34 and 35, channel regions 36 and 37 which are disposed beneath the gate oxide 25 and can be inverted from P-type to N-type by the appropriate application of a bias voltage to the gate 24 in order to permit conduction from the source electrodes 22 and 23 through the inversion layers into the central region disposed beneath the gate 24 and then to the drain electrode 26. (Reference numbers used herein referring to Figure 1 differ somewhat from those in the Lidow et al. disclosure.)

In the central region beneath the gate 24 is located a highly conductive N+ doped region 40 disposed immediately beneath the gate oxide 25. The N+ region 40 has a depth of about $4\mu m$. Region 40 is relatively highly doped compared to the N- doped region immediately beneath it. By making region 40 of relatively highly conductive N+ material by a diffusion

surrounding drift region. This is accomplished prior to formation of the gate electrode itself in the trench, and also prior to forming the source, body and deep body regions.

U.S. Patent No. 4,983,160 issued January 9, 1990, to Blanchard depicts (see Figure 3) a trenched DMOS transistor with an N+ doped region at the lower sides and bottom of the trench. The purpose of this N+ region is to increase breakdown voltage. Hence the doping level of this N+ region is fairly high. Moreover, in this transistor the P+ body regions are much shallower than is the trench, hence there being no parasitic JFET problem.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a prior art planar MOSFET.

Figure 2 shows a transistor in accordance with the present invention.

Figures 3A to 3D shows steps for forming a transistor in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 2 shows a cross-section of a transistor in accordance with the present invention. This cross-section is drawn conventionally and shows only portions of several cells of a typical transistor, which may include thousands of such cells. However, a single cell transistor is also possible. Also, while the present disclosure is directed to a transistor having an N type (N doped) substrate, a P type (P doped) body region and an N type source region, it is to be understood that complementary devices are also possible wherein each conductivity type is reversed.

Also, the cross-sections shown here are not drawn to scale but are intended to be illustrative. While the various transistor doped regions shown here are

$10^{15}/cm^3$. Included as part of body region 56 is a lower deep body P+ doped portion 57 having a total depth from the principal surface of the semiconductor body of about 2.5μm and extending below the bottom of the trenches as shown. A typical doping level of the deep body P+ portion 57 is 2 x $10^{19}/cm^3$.

Penetrating from the principal surface of the semiconductor body into the drift region 54 is a set of trenches which defines the transistor cells. (Only one such trench 62 is shown here, in cross-section.) Trench 62, as are the other trenches, is lined with gate oxide layer 66 which is typically 0.05 to 0.07μm thick, and each trench 62 is then filled with a conductive doped polysilicon gate electrode 64. A typical width of trench 62 is 0.8 to 1.0μ. A typical cell pitch is 6.0μ. A typical depth of trench 62 is 1 to 2μm (less than that of deep body portion 57). Typically therefore the P+ deep body portion 57 extends 0.5μm below the bottom (floor) of the trench 62.

Formed in the upper portion of the epitaxial layer are N+ doped source regions 58, having a typical depth of 0.5μ. A typical doping level of the N+ source regions 58 is 6 x $10^{19}/cm^3$ at the principal surface. Penetrating through the middle of each source region 58 is the trench 62 in which is formed the conductive electrode gate 64. Insulating the upper portion of each conductive gate electrode 64 is a BPSG (borophosphosilicate glass) insulating layer 74 formed over gate electrode 64. Contacting the source regions 58 and body regions 56 is a source-body metallization layer 76.

The depiction herein is of the active portion only of the transistor. Each transistor active portion is typically surrounded by a termination, typically including doped regions and sometimes an additional filled-in trench. Conventional terminations are

34 and 35. Such punchthrough would occur at the principal surface of the P body regions 34 and 35. Thus in the structure of Figure 2, the blocking characteristics are not degraded while advantageously the on-resistance is reduced.

The typical thickness (height) of the trench bottom implant region 70 is 0.5μ. The width is typically that of the trench, i.e. it extends from one side of the trench to the other including the trench corners, and extends a slight distance laterally from the trench corners, as a result of its fabrication by diffusion. A typical distance from the bottom portion of trench bottom implant region 70 to the substrate 50 is 1.0μm, but this distance is not limiting; trench bottom implant region 70 can extend to substrate 50.

An exemplary process flow for fabricating the transistor of Figure 2 is described hereinafter. It is to be understood that this process flow is not the only way to fabricate the structure of Figure 2, but is illustrative. The various parameters given herein may be varied and still be in accordance with the present invention.

One begins as shown in Figure 3A with an N+ substrate 50 conventionally doped to have a resistivity in the range described above. An epitaxial layer 54 is then grown thereon having a higher resistivity (as described above) and a thickness of e.g. 6 to 12μm.

The principal surface of the semiconductor body including the epitaxial layer 54 then has a conventional active mask layer (not shown) formed thereon and patterned. This active mask layer may be oxide or other suitable material, and defines the active portion of the transistor and masks off the termination thereof. It is to be understood that the present figures show only the active portion, with the termination not being shown as being outside the area

Then conventionally a gate mask layer (polymask) is formed over the entire surface of the polysilicon layer and patterned. (This step is not depicted.) This gate mask layer is then used to etch away the polysilicon layer 64, except in the trench 62, and also leaving gate contact fingers (not shown) on the principal surface connecting the gate electrodes in the various trenches.

Then a blanket P-type implant forms the P doped body regions 56 to provide a channel alongside the trench sidewalls. This step uses a dosage of e.g. 10^{13} to 10^{14} per/cm^2 and an energy of 50 to 60 KeV, typically using boron as the dopant for an N channel device.

As depicted in Figure 3D, the combined effects of the P body implant 56 and the P+ tub 57 effectively eliminate the N doped regions 80 of Figure 3C.

Then an N+ source region mask layer is formed and patterned to define the N+ source regions 58. The N+ source region implant is then performed at an energy level of e.g. 60 to 100 KeV at a dosage of 5 x 10^{15} to 8 x 10^{15}/cm^2, the dopant being arsenic. The N+ source mask is then stripped.

Next, a layer of borophosphosilicate glass (BPSG) is conventionally formed (not shown) to a thickness of 1 to 1.5 μm. A BPSG mask layer is then formed and patterned over the BPSG layer, and then the BPSG mask layer is used to etch the BPSG, defining BPSG region 74 of Figure 2 insulating the top side of conductive gate electrode 64.

Then conventional steps are used to complete the device, i.e. stripping the BPSG mask layer, depositing the source-body metal layer, and masking the metal layer to define the source-body contact 76 of Figure 2. Then a passivation layer is formed thereover and a pad mask is formed thereon and patterned to define the pad contacts through the passivation layer. The formation

We claim:

1. A transistor structure comprising:

a substrate of a first conductivity type;

a drift region overlying the substrate and of the first conductivity type and doped to a concentration less than that of the substrate;

a body region of a second conductivity type opposite that of the first conductivity type overlying the drift region, and defining a principal surface of the transistor structure;

a conductive gate electrode extending in a trench from the principal surface through the body region and into the drift region to a depth less than that of the body region;

a source region of the first conductivity type extending into the body region from the principal surface; and

a trench bottom region of the first conductivity type and of a higher doping concentration than the drift region, and extending from a bottom of the trench into the drift region.

2. The transistor structure of Claim 1, wherein the trench bottom region has a doping concentration in a range of $1 \times 10^{16}/cm^3$ to $8 \times 10^{16}/cm^3$.

3. The transistor of Claim 1, wherein the trench bottom region has a doping concentration at least four times that of the drift region.

4. The transistor structure of Claim 1, wherein the body region includes a channel portion in contact with a side of the trench near the principal surface, and a deep body portion more heavily doped than the channel portion and spaced apart from a side of the trench and nearer the bottom of the trench than is the

bottom region; and

forming a source region of the first conductivity type and extending into the body region from the principal surface.

9. The method of Claim 8, further comprising the steps of:

after forming the trench, and before the step of implanting, forming an oxide layer lining the trench; and

etching away at least a predetermined thickness of the oxide layer.

10. The method of Claim 8, wherein the step of implanting comprises implanting negatively charged ions at an energy in a range of 30 to 100 KeV, and a dose of 10^{12} to $10^{13}/cm^2$.

11. The method of Claim 8, wherein the step of implanting comprises directing ions at an angle of 90° to a plane defined by the principal surface.

12. The transistor structure of Claim 8, wherein the trench bottom region has a doping concentration in a range of $1 \times 10^{16}/cm^3$ to $8 \times 10^{16}/cm^3$.

13. The transistor of Claim 8, wherein the trench bottom region has a doping concentration at least four times that of the drift region.

14. The transistor structure of Claim 8, wherein the step of forming a body region comprises:

forming a channel portion in contact with a side of the trench near the principal surface; and

forming a deep body portion spaced apart from a side of the trench and near the bottom of the trench.

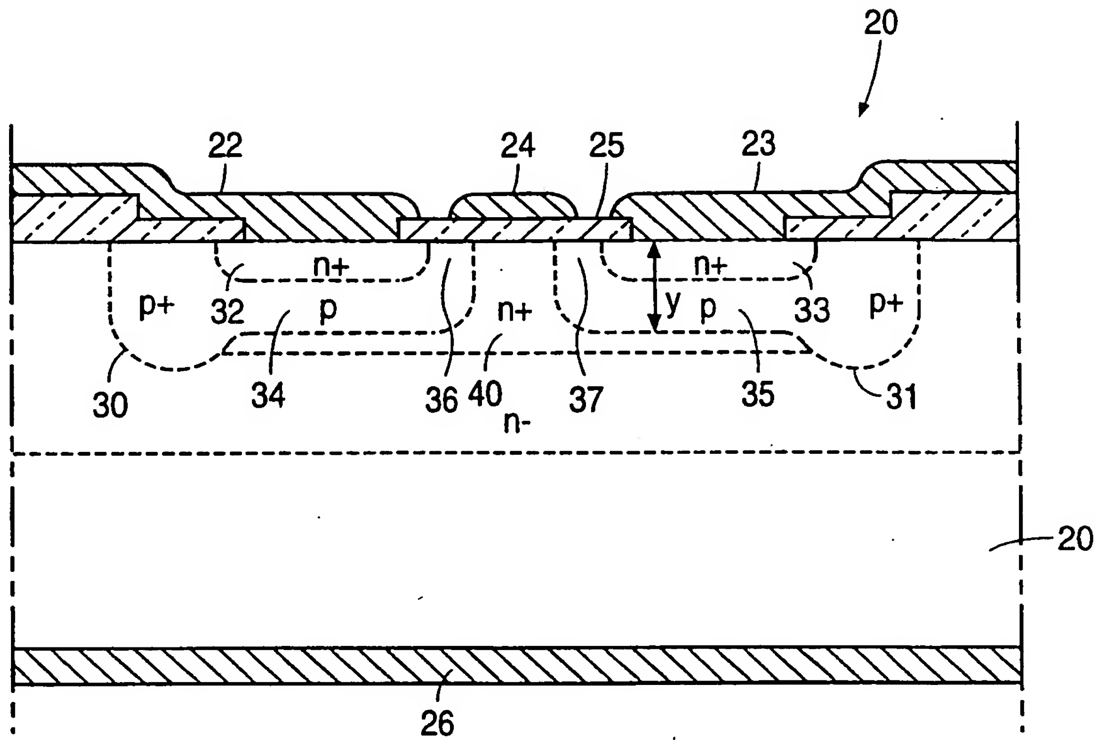


FIG. 1
(PRIOR ART)

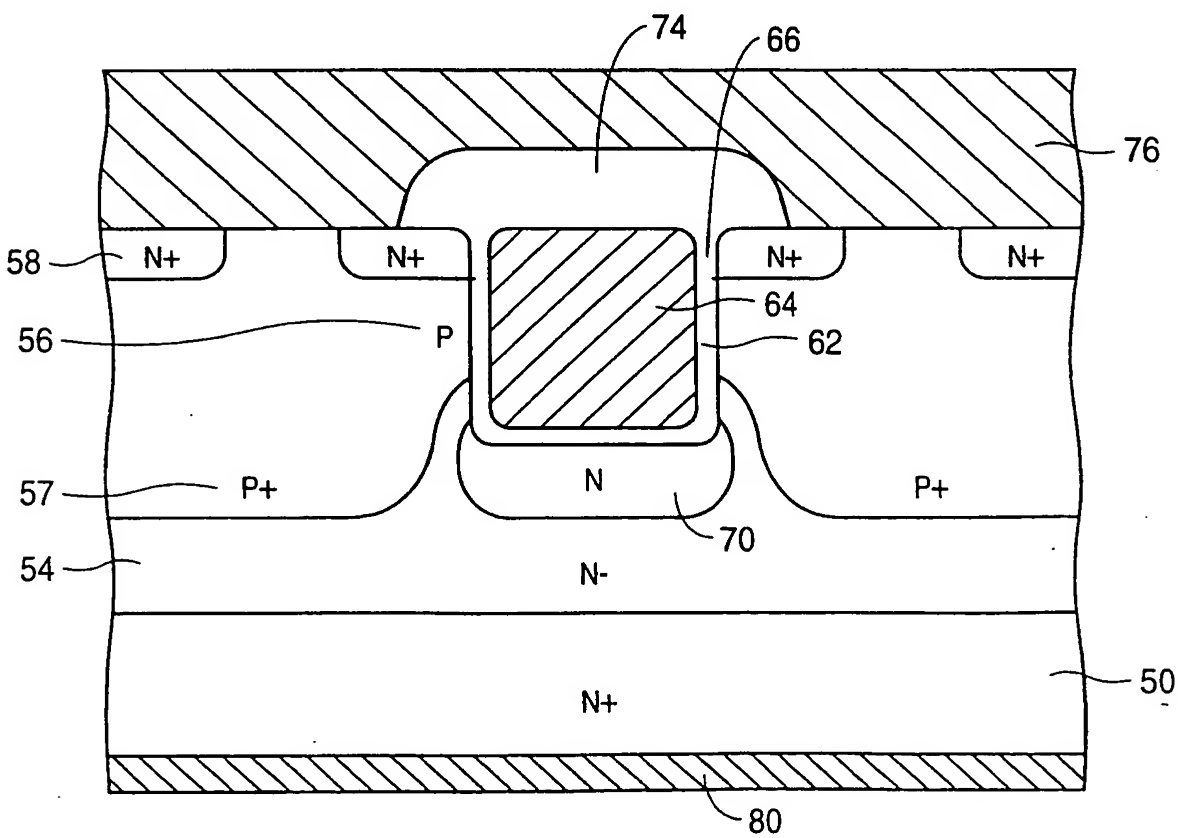


FIG. 2

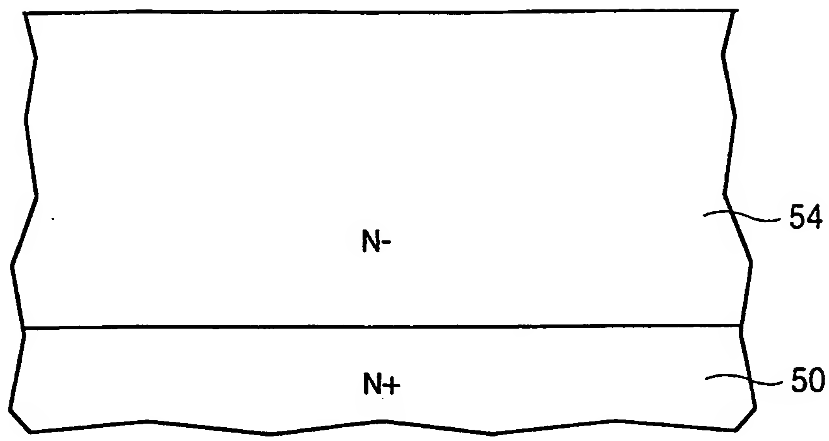


FIG. 3A

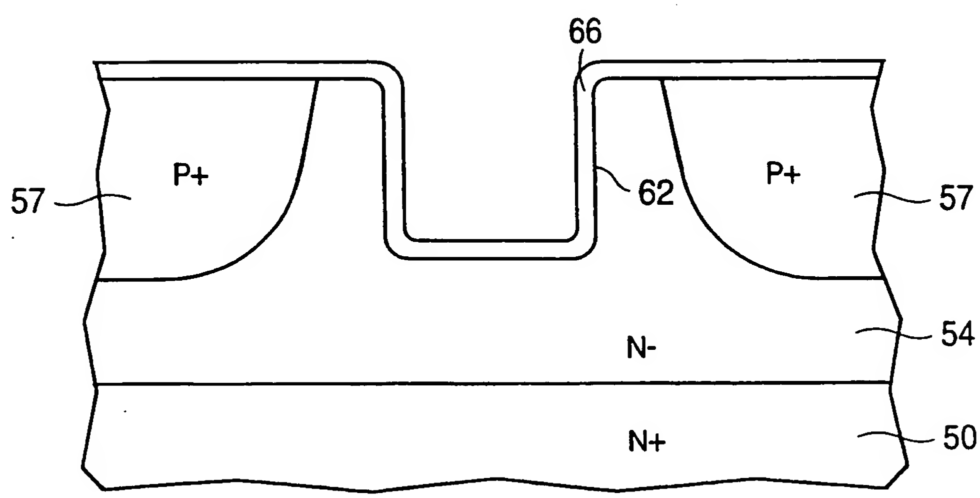


FIG. 3B

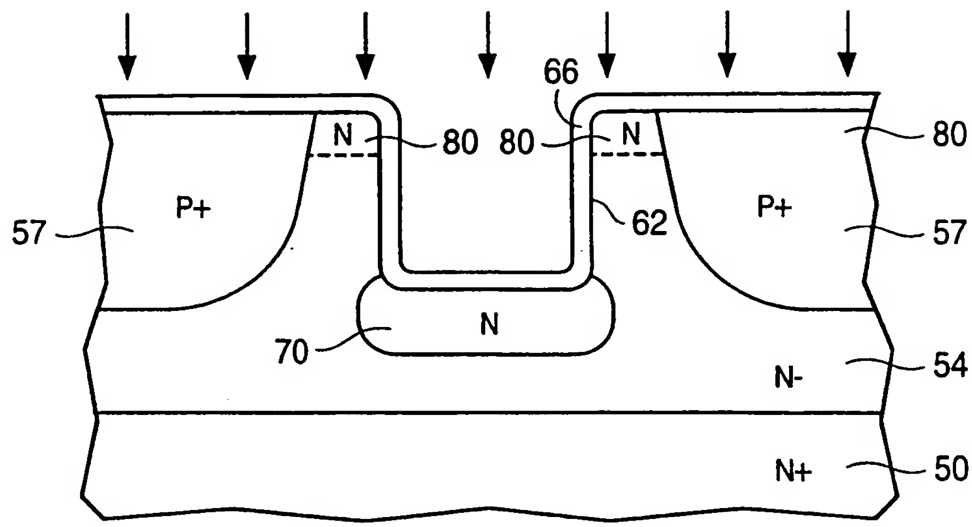
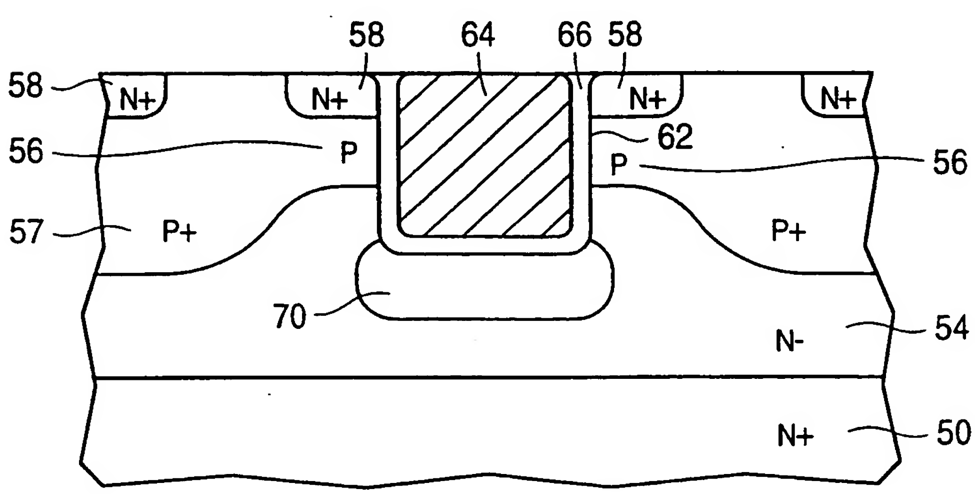

66
80
80
80
N
N
P+
P+
57
57
62
N
70
N-
54
N+
50

FIG. 3C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64
66
58
58
N+
N+
N+
N+
56
P
62
P
56
57
P+
P+
70
N-
54
N+
50

FIG. 3D